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EXAMINER
JEAN GILLES, JUDE

ART UNIT	PAPER NUMBER
2143	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,103	ALLEN ET AL.	
	Examiner	Art Unit	
	Jude J. Jean-Gilles	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Action is in regards to the Reply received on 07/25/2005.

Response to Amendment

1. This action is responsive to the application filed on 01/07/2002. Claim 10 has been amended. Claim 19 and 20 are newly added. Claims 1-20 are pending. Claims 1-20 represent a method and apparatus for a "Fixed snoop response time for source-clocked multiprocessor busses".

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been carefully considered, but are not deemed fully persuasive. Applicant's arguments are deemed moot in view of the following new ground of rejection as explained here below, necessitated by Applicant substantial amendment (i.e., a method wherein fixed snoop response time for source-clocked multiprocessor busses) to the claims which significantly affected the scope thereof.

The dependent claims stand rejected as articulated in the First Office Action and all objections not addressed in Applicant's response are herein reiterated.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Thaller et al (Thaller), U.S. Patent No. 5,555,382 in view of Kato et al (Kato), U.S. Patent No. 6,070,205, further in view of Burns et al (Burns), U.S. Patent No. 6,754,838 B2.

Regarding **claim 1**, Thaller teaches the invention substantially as claimed. Thaller discloses a multiprocessor system comprising:

a first microprocessor having one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock (*fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*);

a memory controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock (*fig. 2, items 18, 106, 114-116; column 6, lines 27-57*); and

However, Thaller does not teach in detail a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the memory controller to the second processor, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal, the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time.

In the same field of endeavor, Kato teaches Burns teaches "...the processor system comprises first and second buses and a plurality of bus masters including a CPU 1301, a Picture Processor 1302, a Sound Processor 1303 and a DMA (Direct Memory Access) controller 1304, all connected to both buses. It also comprises a plurality of bus slaves including an internal memory 1304, and I/O control circuit 1308, a universal timer 1309, and A/D Converter 1310 and an optional DRAM refresh 1315, all connected to the first bus. A first bus arbitrator 1306 and a second bus arbitrator 1307 provide the arbitration for first and second buses respectively. The processor system also include a PLL(Phase Locked Loop) circuit 1311, a clock driver 1312, a low voltage detector 1313 and an external memory interface 1313..." [see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25].

In the same field of endeavor, Burns teaches "...*a system capable of transmitting data to a plurality of processors generating two clock signals, the length of which when traced differ by the amount of tuning etch required to add sufficient delay to the*

forwarded clock signals transmitted to the processors..." [*see Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7 , lines 1-44*].

Accordingly, it would have been obvious to one of ordinary skill in the networking art at the time the invention was made to have incorporated Kato' teachings a second microprocessor connected to the memory controller, with the clock signals of Burns generating the delay, with the teachings of Thaller, for the purpose of "*providing a transmission scheme that offers reliable data transfer between devices while minimizing latency and skew and maximize bandwidth.." as stated by Burns in lines 12-19 of column 3.* Thaller also provides motivation to combine by stating "*providing a bus arbiter that reduces idle time and avoids wastage of bus bandwidth in lines 1-4 of column 5. Kato also provides motivation to combine by stating that there is an option to provide optimization of bus utilization dynamically in lines 36-39, column 4. By this rationale,* ***claim 1*** *is rejected.*

Regarding **claim 2**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus [*see Thaller, fig. 1, items 28, 12; column 6, lines 4-57*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 2 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 2** is rejected.

Regarding **claim 3**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus, and wherein the second interfacing logic does not delay the second signal [*see Thaller, column 53, lines 45-67; column 54, lines 1-42*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 3 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 3** is rejected.

Regarding **claim 4**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus, and wherein the first interfacing logic delays the first signal by a second period of time and the second interfacing logic delays the second signal by a third period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time [see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 4 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 4** is rejected.

Regarding **claim 5**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the memory controller comprises an address switch [*see Thaller, fig. 3A, items 202, 262; column 22 , lines 27-64*]. The same

motivation that was utilized in the combination of claim 1, applies equally as well to claim 5 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 5** is rejected.

Regarding **claim 6**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the first and the second signals carry the same data. [*see Thaller, fig. 1, items 28, 12; column 6, lines 4-57*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 6 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 6** is rejected.

Regarding **claim 7**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal [*see Thaller, items 262; column 8, lines 32-67*];

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock [*see Thaller, fig. 3B, items 232; column 7, lines 4-60*];

a third multiplexer connected to at least the first and the second storage components for receiving the first and the second storage-component output signals and for generating a third multiplexer output signal, the third multiplexer being controlled by a third control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]; and

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and clocked by a third control clock derived from the first system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 7 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 7** is rejected.

Regarding **claim 8**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal [*see Thaller, items 262; column 8, lines 32-67*];

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock[*see Thaller, items 262; column 8, lines 32-67*];

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component

being clocked by a third control clock derived from the second system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a fourth multiplexer connected to at least the first, the second, and the third storage components for receiving the first, the second, and the third storage-component output signals and for generating a fourth multiplexer output signal, the fourth multiplexer being controlled by a fourth control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]; and

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and clocked by a fourth control clock derived from the first system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 8 [*see Burns, column 3, lines 12-19; see Thaller, column 5, lines 1-4*]. By this rationale **claim 8** is rejected.

Regarding **claim 9**, the combination Thaller-Kato-Burns teaches the multiprocessor system of claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal [*see Thaller, items 262; column 8, lines 32-67*];

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-

component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock [*see Thaller, items 262; column 8, lines 32-67*];

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock [*see Thaller, fig. 3 A, items 262; column 8, lines 32-67*];

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component being clocked by a third control clock derived from the second system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a fourth multiplexer configured for receiving the first signal and generating a fourth multiplexer output signal and controlled by a fourth control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and for providing a fourth storage-component output signal to the fourth multiplexer, the fourth storage component being clocked by a fourth control clock derived from the second system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*];

a fifth multiplexer connected to at least the first, the second, the third, and the fourth storage components for receiving the first, the second, the third, and the fourth storage-component output signals and for generating a fifth multiplexer output signal, the fifth multiplexer being controlled by a fifth control signal [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]; and

a fifth storage component connected to the fifth multiplexer for receiving the fifth multiplexer output signal from the fifth multiplexer and clocked by a fifth control clock derived from the first system clock [*see Burns, fig. 4, Mux1; column 6, lines 28-67; column 7, lines 1-67; column 8, lines 1-23*]. The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 9 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 9** is rejected.

Regarding **claim 10**, the combination Thaller-Kato-Burns teaches the multiprocessor system comprising:

a memory controller having one or more interfacing logics including a first interfacing logic, the memory controller being clocked by a first system clock [*see Thaller, fig. 2, items 18, 114-116, 106, column 6, lines 27-57; column 7, lines 4-26*];

a first microprocessor connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the first microprocessor to the first interfacing logic, the first microprocessor being clocked by a second system clock [*see Thaller, fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*); and

a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the second processor to the memory controller, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal [see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25]...".., the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time [*see Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7 , lines 1-44*] . The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 10 [*see Thaller, column 5, lines 1-4; see Kato; column 4, lines 36-39*]. By this rationale **claim 10** is rejected.

Regarding **claim 19**, the combination Thaller-Kato-Burns teaches a system comprising:

a first microprocessor comprising one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock (see Thaller; *fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*);

a memory controller coupled to the first interfacing logic through at least a first high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock (Thaller; *fig. 2, items 18, 106, 114-116; column 6, lines 27-57*);

a second microprocessor comprising one or more interfacing logics including a second interfacing logic, the second microprocessor being clocked by a third system clock see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25];

the second microprocessor coupled to the memory controller through at least a second high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a second signal from the memory controller to the second interfacing logic, the second high frequency, point-to-point, unidirectional, source-clocked bus requiring a first period of time more to transmit the second signal than what the first high frequency, point-to-point unidirectional, source-clocked bus requires to transmit the first signal [see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25]; and

wherein the first interfacing logic is configured to delay the first signal by a second period of time and the second interfacing logic is configured to delay the second signal by a third period of time so that the first signal and the second signal are respectively received by the first microprocessor and the second microprocessor substantially at the same time [*see Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7 , lines 1-44*].

Regarding **claim 20**, the combination Thaller-Kato-Burns teaches the system as recited in Claim 19, wherein the memory controller further comprises one or more interfacing logics including a third interfacing logic and a fourth interfacing logic, and further comprising:

a third high frequency, point-to-point, unidirectional, source-clocked bus coupled to the memory controller and the first microprocessor and configured to transmit at least a third signal from the first microprocessor to the third interfacing logic (Thaller; *fig. 2, items 18, 106, 114-116; column 6, lines 27-57; fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*);

a fourth high frequency, point-to-point, unidirectional, source-clocked bus coupled to the memory controller and the second microprocessor and configured to transmit at least a fourth signal from the second microprocessor to the fourth interfacing logic, the fourth high frequency, point-to-point, unidirectional, source-clocked bus requiring a fourth period of time more to transmit the fourth signal than what the third high frequency, point-to-point, unidirectional, source-clocked bus requires to transmit the third signal [see Kato; fig. 8; column 8, lines 61-67; column 9, lines 1-25]; and

wherein the third interfacing logic is configured to delay the third signal by a fifth period of time and the fourth interfacing logic is configured to delay the fourth signal by a sixth period of time so that the third signal and the fourth signal are respectively received by the memory controller substantially at the same time [*see Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7 , lines 1-44*].

Regarding dependent **claim 11,** claim 11 is substantially the same as **claim 2**, and is thus rejected for reasons similar to those in rejecting **claim 2**.

Regarding dependent **claim 12,** claim 12 is substantially the same as **claim 3**, and is thus rejected for reasons similar to those in rejecting **claim 3**.

Regarding dependent **claim 13,** claim 13 is substantially the same as **claim 4**, and is thus rejected for reasons similar to those in rejecting **claim 4**.

Regarding dependent **claim 14,** claim 14 is substantially the same as **claim 5**, and is thus rejected for reasons similar to those in rejecting **claim 5**.

Regarding dependent **claim 15,** claim 15 is substantially the same as **claim 6**, and is thus rejected for reasons similar to those in rejecting **claim 6**.

Regarding dependent **claim 16,** claim 16 is substantially the same as **claim 7**, and is thus rejected for reasons similar to those in rejecting **claim 7**.

Regarding dependent **claim 17,** claim 17 is substantially the same as **claim 8**, and is thus rejected for reasons similar to those in rejecting **claim 8**.

Regarding dependent **claim 18,** claim 18 is substantially the same as **claim 9**, and is thus rejected for reasons similar to those in rejecting **claim 9**.

Response to Arguments

9. Applicant's Request for Reconsideration filed on November 16th, 2004 has been carefully considered but is not deemed fully persuasive. However, because there exists

the likelihood of future presentation of this argument, the Examiner thinks that it is prudent to address Applicants' main points of contention.

A. The Thaller patent fails to disclose or suggest, a second microprocessor connected to the memory controller through at least a second bus" as recited in Claim 1.

B. Applicant contends that, there is no motivation to combine the teachings of Thaller with the teachings of Burns to approximate the teachings of the present invention. Therefore, as Claim 1 is clearly and precisely distinguishable over the cited Thaller reference in a patentable sense, and there is no motivation to combine Thaller and Burns, Claim 1 is therefore allowable over these references and the remaining references of record.

C. Applicant contends that, New Claims 19 and 20 are allowable for the same reasons as described in points A and B. In particular, neither Thaller, Burns, nor the Examiner's proposed combination of Thaller and Burns disclose the claimed inventions.

10. As to "Point A" it is the position of the Examiner that Thaller teaches the limitations of the above mentioned claims. However, in view of Applicant's remarks, stating that Thaller does not teach a second microprocessor connected to the memory controller through at least a second bus" as recited in Claim 1, new reference of Kato is used to reject this limitation in the claim. Applicant's arguments are deemed moot in view of the above new grounds of rejection as explained above in the rejection of claim 1.

As to "Point B", it is also the Examiner's position that the motivation provided in the first Office action is sufficient to combine Thaller and Burns. Furthermore, new reference of Kato is further used to reject the claimed limitations. See rejection of claim 1 above.

As to "Point C", it is also the Examiner's position new claims 19 and 20 are rejected for the same reasons of the rejection of claim 1 and 10.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from examiner should be directed to Jude Jean-Gilles whose telephone number is (571) 272-3914. The examiner can normally be reached on Monday-Thursday and every other Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley, can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-9000.

Jude Jean-Gilles

Patent Examiner

Art Unit 2143

DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

JJG

October 10, 2005